In the Claims

(Listed in the back)

Applicant has added new claims ~~22-37~~ 33-39 in response to the Examiner's helpful Final Office Action on the Applicant's claims. These claims are presented in response to the Final Office Action and as part of a submission in support of a Request for Continued Examination.

Remarks

Claims 1, 2, 4-7, 14 and 15 were rejected by the Examiner under 35 U.S.C. § 102(e) as being anticipated by Ono (U.S. Patent No. 5,966,606, hereinafter "Ono"). Claims 22-38 as added herein more specifically distinguish over Ono by indicating that trimming requires the reaction of an electrically significant portion of the polysilicon, that only a portion of the polysilicon gate surface may be reacted, and that reaction to a depth of 10 nanometers or more is electrically significant. Ono in contrast, is limited by its claims, as interpreted in light of the specification, to reacting only electrically insignificant depths. Ono's invention gains its electrical significance from preventing the increased depth of penetration of the oxide film inherent in the formation of a bird's beak. Claims 22-38 thus are patentably distinct over Ono, and applicant respectfully submits that claims 22-38 are allowable over the prior art of record in light of the Examiner's rejections.

In addition to the new claims, Applicant respectfully traverses the Examiner's rejections in the Final Office Action with improved (new) arguments as partial submission in support of the RCE.

Traverse to the Rejection on Anticipation Grounds

Per the Examiner, the rejection is maintained as stated in the Office Action mailed June 6, 2001, and as stated below.

The Examiner stated that:

> Applicant argues that Ono does not disclose trimming the gate because it does not alter the electric characteristics of the gate. However, Ono teaches that the characteristics of the gate do change (Column 4, lines 31-33). Furthermore, the characteristics inherently change because the gate is being made smaller.

Applicant traverses as follows: Ono, at column 4, lines 26-32 states:

> Although the nitriding process is conducted at such a high temperature, it is only effected for a short length of time, and accordingly, the profile of boron ions constituting the impurity doped in the channel region does not change during the nitriding step. **That is, the electrical characteristics of the MOSFET do not change significantly after the nitriding step.**

The sentence cited by the Examiner is shown in bold. Applicant respectfully disagrees with the Examiner's interpretation of the language of Ono's patent. Applicant urges the Examiner to see that what this passage is saying is that Ono's process does not significantly change the electrical characteristics of the MOSFET.

Two words may be at issue: "significantly" and "after." Words derive meaning from context. To understand the context of these words, the remainder of Ono's patent must be considered. The central thrust of Ono's invention is to find a process for forming gates that does not produce "bird beaks" because bird beaks change the operational electrical

characteristics of the MOSFET. Ono focuses on avoiding changes to the operational electrical characteristics.

"Significantly"

In that context, the phrase "do not change significantly" should be interpreted to mean "do not change operationally." In device fabrication, changes which affect the operational performance of a device are significant. Changes which do not affect the operational performance of the device are not significant. The alternative interpretation, that the characteristics do change operationally, would have be interpreted as "do change significantly," which is the opposite of what Ono has recited.

Insignificant changes do not anticipate trimming. Trimming involves operationally significant changes in the electrical characteristics, as shown by references to Applicant's specification cited in Applicant's previous Office Action Response. Generally, trimming is a group of methods for changing the operational electrical characteristics of a semiconductor device by changing its size and shape. That trimming involves electrically significant changes is further evidenced by its use for device compensation. A significant change in operational electrical characteristics is inherent in device compensation: the devices are not compensated unless their electrical characteristics change in ways that modify the operational performance of the devices. Applicant urges the Examiner to appreciate the significant electrical changes inherent in trimming for device compensation. That being the case, the Examiner's best response to the independent claim 14, wherein Applicant claims that the "extent of trimming is selected to accomplish device compensation" would be to allow the claim, and those depending from it. Likewise, the Examiner's best response to dependent claim 4, which claims "selectively compensating n-channel and p-channel devices" would be to object to it as depending from an unallowed independent claim, and not to reject claim 4.

"After"

In Ono's phrase, "after the nitriding step," we must inquire as to the prior state to which the word "after" refers. The prior state is the state before Ono's nitriding step. Therefore, in context, the meaning of "after" in this sentence is "during." The context can further be seen from the previous sentence, where "during" is used explicitly to show that the electrically significant portion of the gate, the boron-doped portion, does not change. The Examiner's particular attention is called to Ono's description of the embodiment of Ono's FIGS. 5:

> Although the nitriding step is conducted at such a high temperature, it is only for a short time, and accordingly, the profile of boron ions constituting the impurity ions doped in the channel region does not change in the nitriding step. That is, the electrical characteristics of the transistor do not change significantly **during** the nitriding step. (Ono, col 5, lines 54-60, emphasis added)

Note the parallel language to the passage cited by the Examiner, with the substitution of the word "during" for the word "after." Given that the embodiment of the process in Ono's FIGS. 5 has virtually the same nitriding step as the nitriding step cited by the Examiner, the reasonable conclusion is that both nitriding steps do not change the operational electrical characteristics of the transistor during the nitriding steps.

Ono does not appear to mean "thereafter" by the word "after." While it is true that there are further steps in the process, it is clear that those remaining steps do not change the shape, size, or related electrical characteristics of the gate at all.

Inherent changes

The Examiner's statement that "the characteristics inherently change because the gate is being made smaller" is unsupported. The relevant characteristics are the operational electrical characteristics of the electronic device. Ono has stated that the boron profile does

not change, which raises a presumption that the operational electrical characteristics do not change. Applicant suggests that the Examiner has the burden of presenting evidence that the nitriding step in Ono's method inherently changes the operational electrical characteristics of the gate by changing its size or shape while Ono's method seeks, at every juncture, to avoid such changes. Ono does seek to improve device performance, but the only change Ono seeks is to prevent the formation of bird beaks by coating the exposed edge of the gate oxide with a nitride layer before depositing other oxide material. (Ono, col 5, lines 5-8). Absent the nitride coating in Ono's process, the subsequent deposition of the oxide would expand the edges of the gate oxide to form a bird beak. Ono does not disclose trimming, expressly or inherently, and so does not anticipate Applicant's claims.

Ono's nitride layer

The Examiner also stated that "applicant argues that Ono's nitride layer does not trim an electrically significant portion of the gate. However, the claims are not so limited."

Applicant has added claims which expressly contain the limitation, but wishes to further traverse the Examiner's rejection as to the original claims. The original claims dealing with device compensation (claims 4 and 14) are inherently so limited, as discussed above. Trimming, which is in every original claim, is also inherently so limited. Applicant describes the use of trimming by prior art methods as being to change the operational electrical characteristics of the device, i.e., the speed and the power. (App, p. 2, lines 3-5). Later, Applicant gives a more detailed look at prior art trimming methods: "Conventionally, trimming is accomplished by means of a reactive ion etch (RIE) ash process on a resist pattern before a subtractive etch image transfer into the polysilicon of the gate conductor." (App, p. 7, lines 10-12). Trimming was all about making significant changes to electrical characteristics before Applicant's invention, and is still entirely about making significant electrical changes in Applicant's invention. Applicant has simply invented a better, novel way to accomplish trimming. As further indication, consider Applicant's specification: "In

step 120 of method 100, polysilicon portion 740 may be trimmed to scale down its dimensions so that the resulting gate conductor will be smaller and the associated field effect transistors (FETs) will be **faster and operate at lower power**." (App, p. 5, lines 7-10, emphasis added). Applicant goes on to describe trimming for device compensation as changing the timing (speed) of n-channel devices differently from p-channel devices by "shortening the length of all n-channel devices by one amount and shortening all p-channel devices by another amount." (App, p 5, lines 12 ff) "Trimming" is a term of art that means changing the shape and size of the device in order to change the operational electrical characteristics of the device. Changes to the operational electrical characteristics are significant changes. Changes which do not affect the operational electrical characteristics of the device, such as Ono's superficial nitriding step, are not significant and are not, therefore, the results of "trimming". Because trimming is an element in all of Applicant's claims, all of Applicant's claims should be allowed.

The arguments improved upon above and the new arguments below are, in part, a submission in support of a Request for Continued Prosecution.

"A claim is anticipated only if each and every element as set forth in the claim is found , either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed Cir. 1987). The selective film growth method, which is an element of each of Applicant's claims, is not found, expressly or inherently, in Ono's patent. Applicant's selective film growth method grows the film only on the gate or a portion of the gate where it is needed. The nitriding step of Ono's method grows the film on the entire surface of the transistor, including the gate and substrate, and then etches away the unneeded portion. (Ono, col 4, lines 21-24, lines 37-40, and lines 46-48, Claim 1). Applicant's selective film growth

method does not require etching because the film growth itself, selectively caused only in the areas needed, is sufficient to accomplish trimming. Applicant claims etching in a dependent claim, but unlike Ono's method, etching is not essential to novelty. Because Applicant's selective film growth method is an element of each original independent claim (Claims 1 and 14), and because Ono does not teach selective film **growth**, but only selective film **etching**, the Examiner should conclude that Ono's patent does not anticipate Applicant's claims.

None of the dependent claims are anticipated by Ono because they all include the unanticipated elements of the independent claims, which are "selective film growth" and "trimming."

Because none of the original claims are anticipated by Ono, the Examiner should allow claims 1, 2, 4-7, 14 and 15.

OBVIOUSNESS

Claims 8-10, and 17 were rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Ono (U.S. Patent No. 5,966,606, hereinafter "Ono") in view of Moslehi et al. (U.S. Patent No. 4,715,937, hereinafter "Moslehi").

To establish a prima facie case of obviousness under 35 USC 103(a), the references must teach or suggest all of the claim elements. Here, the references do not teach or suggest all the claim elements in claims 8-10 and 17, and so no prima facie case of obviousness arises for those claims.

Claims 8-10 depend, in sequence, from claim 2. Consequently, the selective nitridation element of each of Claims 8-10 is a variety of Applicant's **selective film growth** method. Likewise, claim 17 contains, through its dependence on claim 15, the element of

selective film growth. Neither Ono nor Moslehi teach, suggest, describe, disclose or even mention selective film growth. Both Ono and Moslehi disclose indiscriminate film growth. Ono teaches growing films over entire transistors, and then teaches selective film etching to remove the unneeded portion. Moslehi describes and claims a process for coating an entire *wafer* at a time, without etching away anything. There is nothing similar to Applicant's selective film growth process in either Ono or Moslehi. Because Ono combined with Moslehi fails to teach or suggest the selective film growth element in the rejected claims, the rejection for obviousness must fail. The examiner should allow claims 8-10 and 17.

Claims 8-10 and 17 contain, through their respective dependencies to their independent claims, the element of trimming. Neither Ono nor Moslehi, nor the two in combination, describe or suggest trimming. "Trimming" is the changing of the shape and size of an electronic device on a chip in order to change its operational electrical characteristics. Ono teaches away from trimming when he describes his nitriding step as not significantly changing the electrical characteristics of the transistor. (Ono, Col 5, lines 54-60). Moslehi never addresses any device-level consequences of his process. Moslehi's process is for putting an insulating layer on a wafer, analogous to a buried oxide layer, except in Moslehi, it is a nitride layer.

Applicant's selective film growth method uses a laser to selectively grow trimming films. (App, claims 8-10 and 17). Ono does not teach a laser and, therefore, Applicant's claims 8-10 and 17 are not obvious in light of Ono alone. Ono's lamp annealing process does not expressly or inherently describe Applicant's laser-heating method because incoherent lamp light does not affect the polysilicon the same way that coherent light, including at 308 nanometers, affects polysilicon. Moslehi mentions, but does not teach, a laser by reference to an article in Applied Physics Letters (Moslehi, Col 2, lines 9-16). However, Moslehi's recited wavelength is 193.7 nanometers (Col 2, line 15) (calculated from the 6.4eV photon as nu = hc/E, where h=planck's constant, c=the speed of light, E is

the energy of the photon, and nu = the wavelength, as derived from fundamental laws E = hf, (where f = frequency) and c = f*nu => f=c/nu, substituting into the first equation for f, and rearranging algebraically), not 308 nanometers. As Applicant points out, the 308 nanometer wavelength is particularly well suited to heat polysilicon and not the surrounding materials. (App, p. 6, line 15 to p.7, line 4). As Moselehi points out, the recited low power laser accomplished its nitridation by generating NH_2 radicals in the atmosphere near the chip surface. (Moslehi, col 2, lines 13-15). Such a process, which relies on creating hot atmospheric radicals to react with the surface, is inherently superficial. Indeed, Moslehi recites films of "less than or equal to 25 angstroms."(Col 2, lines 11-12). A 2.5 nanometer (25 angstrom) film is too superficial to significantly change the shape and size of a device sufficiently to change its operational characteristics, especially at the large device sizes being produced in 1984. Consequently, Moslehi's laser does not suggest the use of a laser for trimming, but only for heating gases for forming superficial films. While Ono and Moslehi could be combined to suggest laser nitriding for superficially coating the edges of gate oxides (and everything else on the chip), there is no suggestion to use Ono and Moslehi for trimming. Both Ono's and Moslehi's teachings, alone or combined, are incapable of enabling the trimming of semiconductor devices. Because Ono combined with Moslehi does not teach Applicant's selective laser heating method for trimming, which is an element of claims 8-10 and 17, Applicant's claims 8-10 and 17 are not obvious in light of Ono and Moslehi.

The Examiner stated that the rejection is maintained as stated in the Office Action mailed June 6, 2001, and as stated below.

The Examiner also stated that "the applicant argues that Moslehi does not teach trimming films with a thickness in the range of 10 nm to 100 nm. However, the claims are not so limited."

Applicant has added claims with relevant limitations, but urges the Examiner to appreciate that original claims 8-10 and 17 are allowable without amendment as argued above. The Applicant's claims are inherently limited to films capable of changing the size and shape of a semiconductor device sufficiently to change the operational electrical characteristics of the device. These limitations are, and always have been, contained in the term of art "trimming."

In summary, none of the references cited by the Examiner nor any other known prior art, either alone or in combination, disclose the unique combination of features disclosed in applicant's claims presently on file. For this reason, allowance of all of applicant's claims is respectfully solicited.

Accordingly, it is respectfully requested that the subject claims, as amended, be reconsidered and allowed.

The amendments herein added 1 new independent claim and 7 dependent claims, resulting in fees due of $206.00. Please deduct this $206.00 fee from deposit account 09-0456. In addition, please deduct any fees or credit any overpayments to deposit account 09-0456.

The Examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Applicants hereby declare that any amendments herein that are not specifically made for the purpose of patentability are made for other purposes, such as clarification, and that no such changes shall be construed as limiting the scope of the claims or the application of the Doctrine of Equivalents.

If any fees, including extension of time fees, are due as a result of this response, please charge IBM Corp Deposit Account No. 09-0456. This authorization is intended to act as a constructive petition for an extension of time, should an extension of time be needed as a

result of this response. The examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Respectfully submitted,

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VERSION OF ALL CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

Claim 1. (Unchanged) A method for forming a trimmed gate in a transistor comprising the steps of:

forming a polysilicon portion of a gate conductor on a substrate having a semiconductor portion; and

trimming the polysilicon portion by a selective film growth method.

Claim 2. (Unchanged) The method of claim 1, wherein the selective film growth method comprises selective surface nitridation.

Claim 3. (Withdrawn) The method of claim 1, wherein the selective film growth method comprises selective surface oxidation.

Claim 4. (Unchanged) The method of claim 1, wherein the step of trimming the polysilicon portion further comprises selectively compensating n-channel and p-channel devices.

Claim 5. (Unchanged) The method of claim 1, additionally comprising the step of at least partially removing the trimming film.

Claim 6. (Unchanged) The method of claim 1, wherein the trimming film is anisotropically etched, forming gate conductor spacers.

Claim 7. (Unchanged) The method of claim 1, wherein the trimming film is silicon-rich and the method further comprises the step of forming additional nitride or oxide layers on the trimming film.

Claim 8. (Unchanged) The method of claim 2, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to 50-1000 expose pulses of laser irradiation with an energy fluence of 200-700 mJ/cm^2 in the presence of ammonia at a pressure of 10-1500 torr.

Claim 9. (Unchanged) The method of claim 8, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 400-500 mJ/cm^2 in the presence of ammonia at a pressure of about 300-500 torr.

Claim 10. (Unchanged) The method of claim 9, wherein ammonia is supplied at about 100 ccm/min.

Claim 11. (Withdrawn) The method of claim 3, wherein the step of trimming the gate conductor by selective surface oxidation comprises exposing structures formed on the semiconductor portion to 50-1000 expose pulses of laser irradiation with an energy fluence of 100-600 mJ/cm^2 in the presence of oxygen at a pressure of 1-760 torr.

Claim 12. (Withdrawn) The method of claim 11, wherein the step of trimming the gate conductor by selective surface oxidation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 200-400 mJ/cm^2 in the presence of oxygen at a pressure of about 100-300 torr.

Claim 13. (Withdrawn) The method of claim 12, wherein oxygen is supplied at about 100 ccm/min.

Claim 14. (Unchanged) A method for forming selectively compensated semiconductor devices comprising the steps of:

forming a plurality of polysilicon portions of gate conductors on a substrate having a semiconductor portion;

masking at least one polysilicon portion intended for a n-channel device;

trimming at least one unmasked polysilicon portion intended for a p-channel device by a selective film growth method, wherein the extent of trimming is selected to accomplish device compensation of the p-channel and n-channel devices.

Claim 15. (Unchanged) The method of claim 14, wherein the selective film growth method comprises selective surface nitridation.

Claim 16. (Withdrawn) The method of claim 14, wherein the selective film growth method comprises selective surface oxidation.

Claim 17. (Unchanged) The method of claim 15, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 400-500 mJ/cm^2 in the presence of ammonia at a pressure of about 300-500 torr.

Claim 18. (Withdrawn) The method of claim 16, wherein the step of trimming the gate conductor by selective surface oxidation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 200-400 mJ/cm^2 in the presence of oxygen at a pressure of about 100-300 torr.

Claim 19. (Withdrawn) A transistor comprising a trimmed polysilicon portion of a gate conductor, wherein the trimming occurred by a selective film growth method.

Claim 20. (Withdrawn) The transistor of claim 19, wherein n-channel and p-channel devices were selectively compensated by the trimming.

Claim 21. (Withdrawn) The transistor of claim 19, wherein a sufficient portion of the trimming film is removed by anisotropic etching to provide gate conductor spacers.

Claim 22. (Withdrawn) The transistor of claim 19, wherein the trimming film is silicon-rich, allowing additional nitride or oxide layers to be formed.

Claim 23. (New) A method for forming a trimmed gate in a transistor comprising the steps of:

forming a polysilicon portion of a gate conductor on a substrate having a semiconductor portion; and

trimming at least an electrically significant portion of the polysilicon portion by a selective film growth method.

Claim 24. (New) The method of claim 23 wherein trimming the polysilicon portion comprises trimming only a portion of the polysilicon portion.

Claim 25. (New) The method of claim 22 wherein trimming at least an electrically significant portion of the polysilicon portion comprises reacting the polysilicon portion to a depth of at least ten nanometers.

Claim 26. (New) The method of claim 22 wherein trimming at least an electrically significant portion of the polysilicon portion comprises reacting the polysilicon portion to a depth within a range of 10 to 100 nanometers.

Claim 27. (New) The method of claim 22, wherein the selective film growth method comprises selective surface nitridation.

Claim 28. (New) The method of claim 22, wherein the step of trimming at least an electrically significant portion of the polysilicon portion further comprises selectively compensating n-channel and p-channel devices.

Claim 29. (New) The method of claim 22, additionally comprising the step of at least partially removing the trimming film.

Claim 30. (New) The method of claim 22, wherein the trimming film is anisotropically etched, forming gate conductor spacers.

Claim 31. (New) The method of claim 22, wherein the trimming film is silicon-rich and the method further comprises the step of forming additional nitride or oxide layers on the trimming film.

Claim 32. (New) The method of claim 27, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to 50-1000 expose pulses of laser irradiation with an energy fluence of 200-700 mJ/cm^2 in the presence of ammonia at a pressure of 10-1500 torr.

Claim 33. (New) The method of claim 32 wherein the laser irradiation is of a wavelength absorbed by the gate material selective to surrounding materials.

Claim 34. (New) The method of claim 32, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 400-500 mJ/cm^2 in the presence of ammonia at a pressure of about 300-500 torr.

Claim 35. (New) The method of claim 34, wherein ammonia is supplied at about 100 ccm/min.

Claim 36. (New) A method for forming selectively compensated semiconductor devices comprising the steps of:

forming a plurality of polysilicon portions of gate conductors on a substrate having a semiconductor portion;

masking at least one polysilicon portion intended for a n-channel device;

trimming at least an electrically significant portion of one unmasked polysilicon portion intended for a p-channel device by a selective film growth method, wherein the extent of trimming is selected to accomplish device compensation of the p-channel and n-channel devices.

Claim 37. (New) The method of claim 36, wherein the selective film growth method comprises selective surface nitridation.

Claim 38. (New) The method of claim 37, wherein trimming comprises reacting the polysilicon portion to a depth of at least ten nanometers.

Claim 39. (New) The method of claim 37, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 400-500 mJ/cm^2 in the presence of ammonia at a pressure of about 300-500 torr.